REMARKS

In accordance with the foregoing, the specification and claims 1, 2, 4-6, 8, 9, 11, 12, 14 and 15 are amended. Claim 7, 10 and 13 are cancelled. New claim 16 is added. Claims 1-6, 8-9, 11-12, 14-15 and 16 remain pending for reconsideration, which is respectfully requested. No new matter is presented and, accordingly, approval and entry of same are respectfully requested.

STATUS OF THE CLAIMS

Claims 1-15 are rejected.

Claims 1, 2, 3, 4, 5, 6, 8, 9, 11, 12, 14, 15 and 16 are pending under consideration.

ITEM 2: SPECIFICATION

The title of the invention, taking into consideration the Examiner's comments, is replaced. Withdrawal of the objection to the title is requested.

ITEM 3: CLAIM OBJECTIONS

Claims 2-8, 10-11 and 13 are objected to because, allegedly, "Claim limitations need to be separated with a semicolon."

It is well accepted to use a comma to separate a wherein clause from another claim recitation. Furthermore, 37 C.F.R. § 1.75(i) states "Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation" and therefore there is no requirement that a wherein clause be separated by a semicolon. However, claims 2, 5, 6 and 11 are amended to improve their form. Withdrawal of the objection to the claims is respectfully requested.

ITEMS 5: REJECTION OF CLAIMS 1-15 UNDER 35 U.S.C. § 102(e)

Claims 1-15 are rejected under 35 U.S.C. § 102(e) as being anticipated by Andou, U.S. Patent Publication No, 2004/0254776, hereinafter referred to as "Andou."

This rejection is respectfully traversed.

At Item 5, page 2, the Office Action cites Andou as disclosing the original claim 1 of the present invention. Particularly, the Examiner cites the Abstract, and paragraphs [0035], [0057], [0059], [0091], [0104], [0121]; [0122], [0123] and [0124] in Andou.

However, Andou fails to disclose or suggest that the timing analysis is performed by accumulating a variation in delay time of each gate in the target path, and only when it is determined that the timing conditions are not satisfied in the first timing analysis, a second timing analysis is performed, based on circuit information and calculated variation coefficients. For example, the Examiner asserts that Andou teaches a determination unit in paragraphs [0121], [0122], [0123] and [0124]. However, applicant disagrees. Andou merely discusses that the propagation delay time Ts is calculated based on the variation coefficient α, corrected with the correction value β, and the propagation delay time Ts, taking into consideration the in-chip variations calculated so as to have the appropriate occurrence whether timing conditions are satisfied or not based on a result of the timing analysis, as set forth in the amended claims 1.

The amended claim 1 recites a first timing analysis unit performing timing analysis in a target path constituting an analysis target, by accumulating a variation in delay time of each gate in the target path (lines 18-22 of page 28; Fig. 7, unit 71); a determination unit determining whether previously specified timing conditions are satisfied or not based on a result of the timing analysis supplied from the first timing analysis unit (lines 22-27 of page 28; Fig. 7, unit 72); a coefficient arithmetically operating unit calculating variation coefficients of delay time in the target path with a variation in delay time in each gate being cancelled out in accordance with a number of gate stages in the target path (lines 5-12 of page 13; lines 7-21 of page 30; Fig. 7, unit 33); and a second timing analysis unit performing timing analysis in the target path based on the calculated variation coefficients by the coefficient arithmetically operating unit (lines 16-22 of page 14; lines 22-28 of page 30; Fig. 7, unit 37).

Accordingly, in the amended claim 1, the first timing analysis is performed by accumulating a variation in delay time in each gate in the target path, and only when it is determined that the timing conditions are not satisfied in the first timing analysis, a second timing analysis is performed, based on circuit information and calculated variation coefficients. As a result, timing analysis with the variation degree in the entire path being reduced according to the number of gate stages can be carried out by extracting only the paths with the rigid timing constraints, and accurate timing analysis can be carried out while reducing the amount of the arithmetic operation processing.

Independent claims 9 and 12 set forth embodiments of the invention with a varying scope and patentably distinguish over the cited prior art for the reasons similar to those discussed above.

Dependent claims are at least patentably distinguishing due to their dependence from the independent claims or recite patentably distinguishing features of their own. Withdrawal of the rejection of pending claims, and allowance of pending claims is respectfully requested.

NEW CLAIM 16

New claim 16 recites:

> 16. (New) A timing analysis apparatus performing timing analysis of a semiconductor integrated circuit based on inputted circuit information, comprising:
>
> a controller,
>
> performing timing analysis in a target path in the semiconductor integrated circuit by accumulating a variation in delay time of each gate in the target path,
>
> determining whether previously specified timing conditions are satisfied based on a result of the performed timing analysis,
>
> performing timing analysis in the target path based on calculated variation coefficients of delay time in the target path with the variation in the delay time of each gate being cancelled out in accordance with a number of gate stages in the target path, only when said timing conditions are not satisfied.

As discussed above, Andou fails to disclose or suggest any of the above features. Thus, claim 16 patentably distinguishes over the cited prior art for the reasons discusses above.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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